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PROGRESS REPORT for Contract N00014-91-J-1518

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"Exploiting Resource Parallelism for Integrated Fault Monitoring and Recovery"

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I. OBJECTIVE

Most emerging high-performance processors, such as superscalar, and VLIW processors, possess substantial fine-grain parallelism in the form of multiple pipeline stages, multiple functional units, and multiple buses. The objective of the proposed research is to develop a new method, called integrated monitoring, which effectively exploits the dynamic availability of parallel resources, e.g. delay slots in the pipe stages or idling functional units, for concurrently detecting program execution errors. Such an approach alleviates the need of a separate and dedicated hardware monitor, and minimizes or eliminates the performance penalty incurred for fault monitoring.

II. PROGRESS

An integrated control flow monitoring method, call Available Resource-driven Control-flow (ARC) method, has been developed and applied to a comercial VLIW processor, the Multiflow TRACE 14/300. Experiments on the TRACE 14/300 indicate that ARC is capable of detecting >99% of the control flow errors while incurring negligible performance penalty. These results demonstrate that ARC is highly effective in using the idling resources of a VLIW processor to achieve concurrent error detection at a very low cost. This work on ARC has resulted in the publication of a paper entitled "Exploiting Instruction-Level Resource Parallelism for Transparent, Integrated Control-Flow Monitoring" in the Proceedings of the Fault Tolerant Computing Symposium, June 1991 (FTCS-21).

As part of the development of ARC, an extensive experimental evaluation of the Multiflow TRACE 14/300 has been performed. The dynamic resource utilization and the degree of instruction level parallelism achieved by this machine have been quantitatively characterized. This effort resulted in the publication of a conference paper entitled "An Instruction-Level

Performance Analysis of the Multiflow TRACE 14/300" in the Proceedings of the MICRO-24 Conference, November 1991. An expanded version of this paper entitled "Instruction-level Experimental Evaluation of the Multiflow TRACE 14/300 VLIW Computer" has been submitted to the special issue of The Journal on Supercomputing on Instruction Level Parallel Processing.

There is also indication that the control-flow monitoring techniques similar to that employed by ARC can be effectively applied to the design of self-monitoring state machines and controllers. Efforts are also underway to explore this promising extension of the signature monitoring research from processors to generalized controllers. Although this is not the primary focus of the proposed research, it constitutes an interesting extension of the primary research effort.

III. RESEARCH PLAN

During 1992, the research effort has been broaden to explore integrated monitoring approaches for superscalar processors. Emerging superscalar processors are capable of fetching, decoding and issuing multiple instructions in every machine cycle. Preliminary indications are that the multiple functional units in superscalar processors exhibit significant number of idling cycles during program execution which can be exploited for concurrent detection of program execution errors. Unlike VLIW's, superscalar processors exploit instruction level parallelism at run time via hardware mechanisms. This makes the development and incorporation of integrated fault monitoring techniques much more difficult and requires more powerful compile-time techniques and tools. Initial progress has been made in the analysis of program execution behavior on the IBM RS/6000, the only widely available workstation that employs a superscalar processor. A profiling tool called "goblin" has been developed that allows the instrumentation of application programs and the collection and analysis of dynamic execution traces. Development of an integrated monitoring technique for the IBM RS/6000 that can be applied to other superscalar processors as well is currently underway.